AMENDMENTS TO THE SPECIFICATION

Please insert a new paragraph at the beginning of the application on page 1, line 1, immediately following the title as follows:

This application is a division of Application No. 10/007,986 filed on 13 November 2001, herein incorporated by reference in its entirety.

Please amend the paragraphs beginning on page 1, line 6 through page 3, line 24 as follows:

In the world of integrated circuits, there are a multitude of electrical connections between the integrated circuits and other integrated circuits and eventually to the "outside world." As integrated circuits become more dense, so must the electrical connections. Integrated circuits are mounted on printed circuit boards and printed-wiring technology is the current method to build circuit-boards having embedded circuit traces. These traces are interconnected with vias/microvias which connects one trace on one circuit-board layer to a trace on a different layer. These vias/microvias, however, degrade the continuity of a signal path introducing variations in the elecrostatic and electromagnetic qualities of the via transition. Varying and controlling the physics of each connection by controlling the dielectric used, the dielectric thickness, and the area of the signal-path can result in a specific, controlled characteristic impedance. Ideally, any portion of any high-density high-speed device should be equally accessed and interconnected with homogenous, impedance-controlled connections to improve signal fidelity with less reflection and reduced ~~electro-magnetic~~

electromagnetic interference. Shielding can be added around the outer portions of the wire to shield against electromagnetic field radiation. There are a myriad of options to provide the electrical connections to/from integrated circuits with these considerations incorporated into the design, such as various small outline packages, plastic leaded chip carrier, dual inline packages, pin grid arrays, ball grid arrays, etc.

The next generation of integrated circuits such as system-on-chip and other high-density devices, however, require high density electrical interconnections. Current limitations of printed-wiring boards have trace widths as small as 0.003 inch. While fine, high-density circuit traces increase the density of a interconnect they also increase the inductance, resistance, and current-carrying ability of the interconnect. High-speed, high-density circuit ~~board~~ boards can be difficult to design if minimum strip-line layers, evenly distributed, with minimum vias are required. In addition, circuit boards ~~for high-speed, high density~~ having exacting high speed and high density requirements can be expensive to manufacture. Previous packaging options, like pin grid arrays and quad flat packs all left something to be desired in achieving these goals. Even with fine line techniques, larger printed circuit board designs have difficulty reaching the inner portions of high-density devices with homogenous, impedance-controlled connections.

An emerging technology that is becoming increasingly popular is to package the high density, high speed integrated devices without any terminations on the bottom.

Such packages are referred to as Land Grid Arrays (LGA). Although not technically accurate, the easiest way to envision an LGA device is to picture a semiconductor with nothing but tiny round gold plated pads on the bottom whereas if the device were a ball grid array, a ball would be soldered to each pad. The biggest reason for terminating a device as an LGA is to achieve higher pin counts (number of outputs) with smaller packages. With new requirements such as high-end printed circuit boards requiring 1000 and more pin counts, even the ball grid array is not an option because the large footprints ~~can not~~ cannot stand the forces on the solder joints that are caused by thermal mismatch, i.e., the materials of the semiconductor device have different coefficients of expansion than those of the target printed circuit board. A "z-axis" connection of the LGA can overcome the thermal mismatch problems.

Land grid arrays offer high interconnection density, e.g., at a one millimeter pitch, a 35 x 35 grid may contain 1,225 interconnections in a space less than 1.5 square inches and 2,025 interconnections in a 45 x 45 grid less than 1.75 square inches. Land grid array modules are easy to manufacture and the cost of module production is ~~must~~ much less because terminations such as pins or balls are no longer required. Recall that it is very important to keep the electrical path of each connection as short as possible for low inductance and the LGA achieves this with a distance from the bottom of the device being socketed to the target board of less than two millimeters with some LGA socket designs. Co-planarity problems are reduced in many instances because LGA sockets

can be manufactured for spring movement of .015" (0.4 mm) which "takes up the slack" when there is a problem with co-planarity on the bottom of the device. LGAs also have low mating force requirements, in some instances requiring only 20 to 35 grams of force per position to achieve reliable mating. When using land grid arrays, moreover, microprocessors can be easily removed and replaced.

Please replace page 8 of the specification as follows:

closest to the array 112 of interconnections 114 and an outer perimeter 122. The dimensions of the sash 120 are such that it provides a meeting and resting area for the frame of an interposer ~~(not shown)~~ 150, the outline of which is represented as a dashed line on Figure 1, that will be placed on the land grid array 112 during interconnection. Preferably, the height of the sash 120 is substantially the same height as the electrical interconnections 114 in order to provide a firm contact and yet seal the array. Note that near the corners of the array 112, the sash 120 is angled 126 to provide smoother coverage and fewer asymptotic electrical fields around the corners. It has been empirically determined that the width of the sash would be at least sufficient to prevent the variations of current density occurring at the electrical interconnections 114 during deposition, i.e., creation of the electrical interconnections.

Electrical connections 116 may be provided intermittently at the periphery of the array 112 to electrically connect the sash 120 to a logic ground or other electrical

interconnection 114. This feature is optional but is preferred in that the sash 120 may be electrically tied to a voltage V_N 140 which may be at the frame voltage or printed circuit card ground voltage or some other voltages. The electrical connections 116 thus provide a redundant and low impedance connection to the sash. These redundance intermittent electrical connections 116 also offer some advantageous repair features when similar designs are incorporated onto the non-contact side of the carrier having the LGA, as disclosed in U.S. Patent Application Serial No. 09/852,998 entitled *Land Grid Array (LGA) Pad Repair Structure and Method* filed on 10 May 2001, owned by a common assignee, and herein incorporated by reference in its entirety. Although shown in the ~~figure~~ figures as extending towards and ~~connected~~ connecting the electrical interconnections 114 to the sash 120, the electrical connections 116 may actually extend in another direction to electrically connect capacitors or other circuit devices 136 included on the carrier ~~(not shown)~~ to a bias or voltage other than that of the electrical interconnections 114. These electrical ~~interconnects~~ connections 116 thus may provide electrical design flexibility for interconnection and grounding schemes of housings or other components as well.